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ART UNIT	**PAPER NUMBER**
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,453	JOSHI ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-19 and 33-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-19 and 33-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/8/07 has been entered.

Response to Arguments

Applicant's arguments filed 6/8/07 have been fully considered but they are not persuasive. Two arguments were presented and they are discussed below.

The first argument is that Shibata fails to teach a bond pad. The rejections reliance upon the second terminal [61] as the claimed bond pad is traversed because Shibata earlier teaches the second terminals [21] are obtained by plating the wiring patterns with nickel and gold. With this in mind, the rejection fails to substantiate how Shibata teaches a bond pad.

Please note, skilled artisans would agree that the term "terminal" is another word for "bond pad", especially in view of the drawings and use of the terminal in Shibata. Further, a bond pad is an area on a chip or substrate where a wire or solder ball is

attached in order to electrically connect the chip or substrate to another chip or substrate. Therefore, the terminal of Shibata meets the definition of a bond pad.

The second argument is that there is no motivation to combine the teaching of Kaneda with Shibata because Kaneda teaches uses heat bonding while Shibata uses ultrasonic bonding. The heat bonding of Kaneda must be used in order to melt the insulator allowing for an electrical connection to be made and the ultrasonic bonding of Shibata fails to provide heat.

Please note that the method used for bond is unimportant. Shibata doesn't teach any importance or limiting factor to the bonding method, therefore it would have been obvious to one of ordinary skill in the art to use any known equivalent bonding method, such as heat bonding. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950). When using the claimed adhesive material, a skilled artisan knows that heat is required to make it work. Therefore, using a heat bonding in place of ultrasonic bonding is readily apparent and more than obvious to a skilled artisan. Also, note that applicant is reading process limitations into a product claim. The rejection shows that conductive particles comprise metal with an insulating layer is known to skilled artisans.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1, 2, 4, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890 in view of Kaneda et al., US Patent 6,223,429.

Shibata (Figures 5 & 6) teaches a wafer-level chip scale package, comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 2, Shibata teaches at least one conductive particle is located between the stud bump and the bond pad (figure 6).

With respect to claim 4, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

As to claim 5, Shibata teaches the chip contains an integrated circuit in communication with a chip pad (7, 44+).

In re claim 7, Shibata, which teaches the bump is made of gold (7, 45+), teaches the package does not contain any solder paste.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, as applied to claim 1 above, and further in view of Applicant's admitted prior art APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, as applied to claim 1 above.

Regarding claim 8, while Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp II-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

With respect to claim 9, while Shibata fails to teach the stud bump is a coined stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a coined stud bump in the invention of Shibata because the use of a stud bump or a coined stud bump are equivalent. A skilled artisan knows that each are commonly known and used bumps to interconnect a die to a substrate, as taught by Lau, Flip Chip Technologies, 1996, pp. 129-131. The substitution of one known

equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 10, while Shibata fails to teach the chip does not contain a chip pad overlying an integrated circuit (IC), this is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). Placement of the chip pad relative to the IC is known to a skilled artisan since placing it away from the chip pad protects the IC from the heat and pressure put upon the pad.

Claims 11, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches a wafer-level chip scale package, comprising:

a chip [10] containing a stud bump [11];

a substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad.

While Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the

art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp 11-207. The substitution of one known equivalent technique .for another may be obvious even if the prier art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Further, Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 12, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 14, Shibata, which teaches the bump is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 11 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claims 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches a wafer-level chip scale package, comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad.

While Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu

are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp 11-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Further, Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 16, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 18, Shibata, which teaches the bump is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 15 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches an electronic apparatus containing a packaged semiconductor device without solder paste (7, 45+), the device comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] contacting both the chip and the substrate.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Claims 33, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata teaches a wafer-level chip scale packaged semiconductor device, the device comprising:

a chip [10] containing a stud bump [11];

a substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 34, Shibata teaches the adhesive material' comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 36, Shibata, which teaches the bump. is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 33 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claims 37, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (Figures 5 & 6) teaches an electronic apparatus containing a wafer-level chip scale packaged semiconductor device, comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 38, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 40, Shibata, which teaches the bump is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim 39 is rejected Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 37 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claims 41,42, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches a wafer-level chip scale package without solder paste (7, 45+), comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate, wherein a conductive particle contacts both the stud bump and the bond pad.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to Use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 42, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 44, while Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp II-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 45, while Shibata fails to teach the stud bump is a coined stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a coined stud bump in the invention of Shibata because the use of a stud bump or a coined stud bump are equivalent. A skilled artisan knows that each are commonly known and used bumps to interconnect a die to a substrate, as taught by Lau, Flip Chip Technologies, 1996, pp. 129-131. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144

USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 41 above and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/
Primary Examiner
August 7, 2007